



US 20090315083A1

(19) **United States**(12) **Patent Application Publication****Pan et al.**(10) **Pub. No.: US 2009/0315083 A1**(43) **Pub. Date: Dec. 24, 2009**(54) **STRUCTURE AND METHOD FOR FORMING
A THICK BOTTOM DIELECTRIC (TBD) FOR
TRENCH-GATE DEVICES**(76) Inventors: **James Pan**, West Jordan, UT (US);
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H01L 29/00 (2006.01)
H01L 21/76 (2006.01)
(52) **U.S. Cl.** **257/280; 438/426; 257/E21.54;
257/E29.001**(57) **ABSTRACT**

A semiconductor structure which includes a trench gate FET is formed as follows. A plurality of trenches is formed in a semiconductor region using a mask. The mask includes (i) a first insulating layer over a surface of the semiconductor region, (ii) a first oxidation barrier layer over the first insulating layer, and (iii) a second insulating layer over the first oxidation barrier layer. A thick bottom dielectric (TBD) is formed along the bottom of each trench. The first oxidation barrier layer prevents formation of a dielectric layer along the surface of the semiconductor region during formation of the TBD.

